PRIMARY-SIDE CONTROLLED FLYBACK POWER CONVERTER

BACKGROUNDING OF THE INVENTION

Field of Invention

[0001] The present invention relates to a switching mode power converter and more particularly relates to a flyback power converter.

Description of Related Art

[0002] A flyback power converter typically includes a PWM controller, a power MOSFET (Metal Oxide Semiconductor Field Effect Transistor), a transformer, and a feedback-control circuit. The purpose of the feedback-control circuit is to sense the output voltage and/or the output current of the secondary-side of the power supply, and to supply a feedback signal to the PWM controller through an isolated device such as an optical-coupler.

[0003] FIG. 1 shows a traditional flyback power converter. Although this circuit is able to regulate the output voltage and output current, it has several drawbacks. One drawback of this circuit is its large size, due to the need for an optical-coupler and a secondary feedback-control circuit. Another drawback of this flyback power converter is high power consumption. To maintain a constant secondary-side output current, this circuit includes a current-sense resistor. The current-sense resistor significantly increases the power consumption of the power converter.

[0004] In recent years, several primary-side control schemes for flyback power converters have been proposed. These prior-art primary-side control schemes have attempted in various ways to reduce the size and the cost of flyback power converters.

One prior-art primary-side control scheme is "Switching Power Supply Packages" by Arthur J. Collmeyer, Mark D. Telefus, Dickson T. Wong, and David B. Manner (U.S. Pat. No. **6,434,021**). Although this circuit is able to regulate the output voltage and the output current, it has several drawbacks. One drawback of this prior-art invention is that the feedback control voltage is sensed from a high voltage source. This method results in a loss of accuracy, and it increases the cost of the controller. Another drawback is that the voltage drop of the output rectifier is not compensated for. Generally, the voltage drop of the output rectifier decreases in response to temperature increases, typically at a rate of 2mV/°C. Thus, the output voltage of this prior-art invention will deviate significantly from a constant DC level.

[0005] Another prior-art control scheme is "Method and Apparatus Providing a Multi-Function Terminal for a Power Supply Controller" by Balu Balakrishnan, Alex B. Djenguerian, and Leif O. Lund (U.S. Pat. No. **6,538,908**). The drawback of this prior-art is that the optical-coupler and the secondary feedback circuit are still required for loop control. Otherwise, the output voltage and the output current will fluctuate significantly.

[0006] Reflected voltage control has also been proposed as a means for primary-side control. Two prior-art patents teaching this method include "Switched Mode Power Supply Responsive to Voltage across Energy Transfer Element" by Balu Balakrishnan, David Michael, and Hugh Matthews (U.S. Pat. No. **6,233,161**) and "Switched Mode Power Supply Responsive to Current Derived from Voltage across Energy Transfer Element Input" by Balu Balakrishnan, David Michael, and Hugh Matthews (U.S. Pat. No. **6,480,399**).

[0007] One principal drawback of these two prior-arts is inaccurate feedback control. In order to generate a feedback control signal, the reflected voltage of the transformer is

filtered and turned into a DC voltage (or current) through a resistor-capacitor circuit. However, this reflected voltage signal is not directly proportional to the output voltage, because of the spike voltage generated by the leakage inductance of the transformer. Thus, the output voltage of this prior-art invention will deviate significantly from a constant DC level. Furthermore, the voltage drop of the output rectifier is not compensated for in the feedback loop. When load changes occur, this problem will introduce additional distortion into the output voltage.

[0008] Another drawback of these two prior-art inventions is high power consumption. The reflected voltage is filtered to supply power for PWM control. However, the resistor in the filter burns the majority of the reflected power, even if the power consumption required for PWM control is low. Therefore, the power consumption of the power supply is high.

[0009] Thus, a need still remains for an efficient primary-side flyback power converter with a well regulated, constant, output voltage and output current.

SUMMARY OF THE INVENTION

[0010] A principal object of the present invention is to provide a flyback power converter under primary-side PWM control. The flyback power converter according to the present invention supplies a well-regulated constant voltage and constant current output. However, unlike prior-art PWM controllers, it does not require a secondary-side feedback circuit or an optical-coupler. This enables the device count, the size, and the cost of the power supply to be reduced.

[0011] A further object of the present invention is to solve the drawbacks of the foregoing prior-art inventions.

[0012] A further object of the present invention is to reduce power consumption. To achieve this, the present invention provides a PWM controller with a power supply that has a low-voltage source.

[0013] A further object of the present invention is to improve the DC output voltage accuracy and reduce the cost of the PWM controller. To achieve this, the present invention uses a low voltage input to detect the output voltage.

[0014] Another object of the present invention is to further improve DC output voltage accuracy. The present invention includes a double sample amplifier that precisely acquires a sampled voltage from a flyback voltage of the transformer, in a manner such that the sampled voltage is compensated and tightly-correlated to the output voltage.

[0015] The primary-side PWM controller according to the present invention can provide a well-regulated output voltage and output current. This allows the device count, the size, and the cost of the power converter to be greatly reduced.

[0016] The flyback power converter according to the present invention includes the PWM controller that generates a PWM signal to drive a switching transistor. The PWM signal is generated in response to the sampled voltage.

[0017] The flyback energy from the primary winding of the transformer is recycled to reduce power consumption. After the falling-edge of the PWM signal, the flyback energy of the primary winding is rectified and filtered to supply DC power to the PWM controller. This flyback energy includes the flyback voltage reflected from the secondary winding and an induced voltage caused by the leakage inductance.

[0018] Another feature of the flyback power converter according to the present invention is a pulse generator. The pulse generator of the PWM controller generates sampling pulses after each delay time interval. The sampling pulses are used to

accurately detect the flyback voltage of the transformer. The delay time is inserted to avoid interference from the induced voltage created by the leakage inductance of the transformer. The double sample amplifier samples the flyback voltage just before the amplitude of the transformer current falls to zero. This method of sampling compensates for load-related voltage variations across the output rectifier.

[0019] Another feature of the flyback power converter according to the present invention is an offset current source. The offset current source is used to compensate for the temperature dependence of the output rectifier. This allows the PWM controller to be supplied with a more accurate feedback signal. The offset current source of the PWM controller pulls an offset current from an input of the double sample amplifier in response to the operating temperature of the flyback power converter. The offset current will produce a voltage drop across a detection resistor to compensate for voltage variations across the output rectifier.

[0020] Another feature of the flyback power converter according to the present invention is a blanking circuit. The blanking circuit produces a blanking time to ensure that the on-time of the PWM signal will create a sufficient delay to precisely sample the flyback voltage.

[0021] Another feature of the flyback power converter according to the present invention is the use of an oscillator in the PWM controller to produce a programmable switching frequency. The programmable switching frequency is produced in response to the voltage sampled from the flyback voltage. The programmable switching frequency is used by the flyback power converter to control the amount of power delivered from the primary-side of the transformer to the output of the power converter.

[0022] It is to be understood that both the foregoing general descriptions and the

following detailed descriptions are exemplary, and are intended to provide further explanation of the invention as claimed. Still further objects and advantages will become apparent from a consideration of the ensuing description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0024] FIG. **1** shows a traditional prior-art flyback power converter.

[0025] FIG. **2** shows a primary-side controlled flyback power converter according to the present invention.

[0026] FIG. **3** shows a preferred embodiment of a PWM controller according to the present invention.

[0027] FIG. **4** shows a preferred embodiment of a double sample amplifier of the PWM controller according to the present invention.

[0028] FIG. **5** shows a preferred embodiment of a programmable current generator of the double sample amplifier according to the present invention.

[0029] FIG. **6** shows a preferred embodiment of an oscillator of the PWM controller according to the present invention.

[0030] FIG. **7** shows a preferred embodiment of a PWM circuit of the PWM controller according to the present invention.

[0031] FIG. **8** shows a preferred embodiment of a blanking circuit of the PWM circuit according to the present invention.

[0032] FIG. **9** shows a preferred embodiment of a pulse generator of the PWM controller according to the present invention.

[0033] FIG. **10** is a timing diagram showing signals generated by the PWM circuit and the flyback power converter according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0034] FIG. **1** shows a traditional flyback power converter. A capacitor **34** is connected to a PWM controller **90** and is charged via a resistor **22**. The PWM controller **90** will be started up once its supply voltage V_{CC} is higher than a start-threshold voltage. When the PWM controller **90** starts to operate, it will output a PWM signal to drive a switching transistor **80** and a transformer **40**. Meanwhile, an auxiliary winding N_A of the transformer **40** supplies the supply voltage V_{CC} via a rectifier **14**. A current-sense resistor **25** converts a switching current of the transformer **40** into a voltage signal for PWM control and over-power protection. An output of an optical-coupler **92** supplies a feedback voltage V_{FB}.

[0035] The output voltage V_O and the Zener voltage of a Zener diode **96** drive an input of the optical-coupler **92** via a resistor **28** to form the feedback loop. The magnitude of the feedback voltage V_{FB} of the PWM controller **90** determines the on-time (T_{ON}) of the PWM signal and regulates the output power. A transistor **84** coupled with a current-limit resistor **86** control the maximum amplitude of the output current I_O. As the output current I_O increases, the voltage across the current-limit resistor **86** increases as well. When this voltage exceeds the junction voltage of the transistor **84** (e.g., 0.7V), the transistor **84** will be turned on. This reduces the on-time of the PWM signal by decreasing the feedback voltage V_{FB}. In this manner, the output current I_O of the power supply is kept constant.

[0036] FIG. **2** shows a flyback power converter according to the present invention. The flyback power converter supplies a constant output voltage and a constant current output under primary-side PWM control. An input V_{IN} of the power converter is connected to a drain of a switching transistor **80**. A first primary winding N_{P1} and a second primary winding N_{P2} are connected in series to construct a primary winding of a transformer **50**. A first terminal of the primary winding is a first terminal of the first primary winding N_{P1}, and a second terminal of the primary winding is a second terminal of the second primary winding N_{P2}. A second terminal of the first primary winding N_{P1} is connected to a first terminal of the second primary winding N_{P2}. The transformer **50** further comprises a secondary winding N_S.

[0037] The secondary winding N_S of the transformer **50** is connected to an output of the power converter via an output rectifier **19**. A source of the switching transistor **80** is connected via a current-sense resistor **25** to the first terminal of the primary winding of the transformer **50**. The second terminal of the primary winding is connected to the ground reference. When power is applied to the input V_{IN} of the power converter, a capacitor **35** is charged up via a start-up resistor **20**. The capacitor **35** is connected to a supply-voltage input **VCC** of a PWM controller **100**. The capacitor **35** stores energy that is used by the PWM controller **100**.

[0038] Once the voltage at the supply-voltage input **VCC** of the PWM controller **100** exceeds the start-threshold voltage, the PWM controller **100** will start to operate and generate a PWM signal V_{PWM}. The PWM signal V_{PWM} will drive a gate of the switching transistor **80** to deliver energy to the output of the power converter. At the instant the PWM signal turns off, a flyback voltage will be reflected from the secondary winding N_S to the first primary winding N_{P1} and the second primary winding N_{P2}. The voltage across

the secondary winding N_S is equal to the sum of the voltage drop across the output rectifier **19** and the output voltage V_O of the power converter.

[0039] The PWM controller **100** has a detection input **VS** for sampling the flyback voltage V_{P1} from the first primary winding N_{P1}. This is used to regulate the output voltage V_O. The PWM controller **100** regulates the output voltage of the power converter by modulating the PWM signal V_{PWM} in response to the voltage sampled at the detection input **VS**. While the PWM signal V_{PWM} is on, a primary current of the transformer **50** will produce a current-sense voltage V_{IS} across the current-sense resistor **25**. A capacitor **37** is connected from the COM input of the PWM controller **100** to the ground reference. The capacitor **37** is used for frequency compensation to stabilize the control loop of the power converter.

[0040] A sense-junction connects the source of the switching transistor **80** and the current-sense resistor **25**. The sense-junction is connected to a current-sense input **IS** of the PWM controller **100**. The current-sense input **IS** detects the current-sense voltage V_{IS}, so that the PWM controller **100** can successfully limit the peak value of the primary current flowing through the transformer **50**.

[0041] An anode of a diode **15** is connected to the second terminal of the first primary winding N_{P1}. A cathode of the diode **15** is connected to the supply-voltage input **VCC** of the PWM controller **100**. After the PWM signal V_{PWM} turns off, the rectified flyback voltage of the first primary winding N_{P1} is supplied to the supply-voltage input **VCC** of the PWM controller **100** via the diode **15**. The capacitor **35** filters this rectified flyback voltage to supply the PWM controller **100** with a DC power source.

[0042] One component of the voltage supplied to the supply-voltage input **VCC** of the PWM controller **100** is from the flyback voltage reflected from the secondary winding N_S.

However, the voltage supplied to the supply-voltage input **VCC** of the PWM controller **100** also includes an induced voltage from the leakage inductance of the transformer **50**. This flyback energy of the first primary winding N_{P1} of the transformer **50** is recycled to power the PWM controller **100**, thus reducing power consumption.

[0043] The flyback energy of the second primary winding N_{P2} of the transformer **50** is not utilized. Consequently, to eliminate the induced voltage caused by the leakage inductance of the second primary winding N_{P2} of the transformer **50**, a snubber circuit is connected in parallel with the second primary winding N_{P2}. The snubber circuit comprises a diode **17** connected in series with a voltage-clamping device **47**. The voltage-clamping device can either be a Zener diode or a TVS (Transient Voltage Suppressor).

[0044] FIG. **3** shows a preferred embodiment of the PWM controller **100** including a double sample amplifier (DSA) **200**, an oscillator **300**, a PWM circuit **500**, a pulse generator **700**, a zero current detection (ZCD) comparator **900**, and a threshold voltage **910**. When the PWM signal V_{PWM} is off, the pulse generator **700** generates a sampling pulse V_{SP1} and a sampling pulse V_{SP2} alternately. The sampling pulse V_{SP1} and the sampling pulse V_{SP2} are generated following a delay time T_d. The delay time T_d is chosen such that the flyback voltage of the first primary winding N_{P1} of the transformer **50** can be sampled. The delay time T_d is needed to avoid sampling the induced voltage from the leakage inductance of the transformer **50**.

[0045] Once the ZCD comparator **900** detects a zero current status from the transformer **50**, the pulse generator **700** will be inhibited to generate the sampling pulse V_{SP1} and the sampling pulseV_{SP2}. In the mean time, the feedback signals sampled during the sampling pulses V_{SP1} and V_{SP2} are stored in a signal buffer of the double sample amplifier **200**.

[0046] Before initiating the next switching cycle, the pulse generator **700** will produce a sampling pulse V_{SP3} for acquiring a sampled voltage V_{SH} from the signal buffer. In response to the sampled voltage V_{SH}, the double sample amplifier **200** will generate a clamped-sample voltage V_{HSH} for supplying to the oscillator **300**. In order to eliminate the possibility of sampling a falling edge signal, only the higher voltage in the signal buffer is taken as the sampled voltage V_{SH}. The available sampled voltage V_{SH} is acquired just before the transformer current drops to zero. More specifically, the available sampled voltage V_{SH} is acquired when the current of the secondary winding N_S of the transformer **50** drops to a minimum value. Sampling the flyback voltage V_{P1} during a minimum secondary current reduces the error margin from the voltage drop of the output rectifier **19**. The ZCD comparator **900** outputs a ZCD signal V_{ZCD} to indicate a zero current status once the voltage at the detection input **VS** drops below a lower-limit voltage. The lower-limit voltage is the threshold voltage **910** plus an output voltage V_H of the signal buffer. The flyback voltage V_{P1} is sampled through a detection resistor **23** shown in FIG. **2**.

[0047] The sampled voltage V_{SH} is used for voltage regulation. One problem is that the voltage drop across the output rectifier **19** varies with respect to temperature. In order to compensate for this, an offset current source of the PWM controller **100** pulls an offset current I_M from the detection input **VS**. The offset current I_M is decreased in proportion to the increase of the temperature. The offset current I_M produces a voltage drop across the detection resistor **23** so that the voltage drop is proportional to the voltage drop across the output rectifier **19**. By properly selecting the resistance of the detection resistor **23**, it is possible to accurately offset the variation of the voltage drop across the output rectifier **19**. When the variation of the voltage drop across the detection resistor **23** is correlated to the

variation of the voltage drop across the output rectifier **19**, the detection resistor **23** can adequately compensate for the temperature coefficient of the output rectifier **19**. In this manner, the flyback power converter according to the present invention can supply a well-regulated output voltage over a wide range of operating temperatures.

[0048] As shown in FIG. **3**, the oscillator **300** of the PWM controller **100** produces the programmable switching frequency in response to the clamped-sample voltage V_{HSH}, and thus controls the power delivered from the primary-side of the transformer to the output of the power converter. The clamped-sample voltage V_{HSH} is correlated to the output voltage V_O. Thus, the switching frequency will vary in proportion to the output voltage V_O. With a programmable switching frequency, the flyback power converter according to the present invention can maintain a constant output current I_O.

[0049] The PWM controller **100** generates the PWM signal V_{PWM} from a feedback voltage V_{COM}, a limit voltage V_{LIMIT}, and the current-sense voltage V_{IS}. The PWM signal V_{PWM} is used for PWM control. The PWM signal is generated such that the output voltage and the output current are both well regulated.

[0050] FIG. **4** shows a preferred embodiment of the double sample amplifier **200** of the PWM controller **100** according to the present invention. In this embodiment, the detection input **VS** is connected to an input terminal of a switch **220** and to an input terminal of a switch **221**. The switch **220** is turned on/off by the sampling pulse V_{SP1}. An output terminal of the switch **220** is connected to a capacitor **230** to produce a hold voltage V_{H1}. The capacitor **230** is further connected to a positive terminal of an operational amplifier **246**. The switch **221** is turned on/off by the sampling pulse V_{SP2}. An output terminal of the switch **221** is connected to a capacitor **231** to produce a hold voltage V_{H2}. The capacitor **231** is connected in parallel with a switch **225**. The PWM

signal V_{PWM} will control the switch **225** to discharge the capacitor **231** during each switching cycle. The capacitor **231** is further connected between a positive terminal of an operational amplifier **245** and the ground reference. The operational amplifier **245,** the operational amplifier **246,** the capacitor **230,** the capacitor **231,** a diode **266,** and a diode **265** develop the signal buffer of the double sample amplifier **200.** The signal buffer outputs the voltage V_H. Via the diodes **266** and **265,** an output of the operational amplifier **246** and an output of the operational amplifier **245** are connected to the output of the signal buffer. A negative terminal of the operational amplifier **246** and a negative terminal of the operational amplifier **245** are also connected to the output of the signal buffer. Therefore, the magnitude of the signal buffer output voltage V_H is equal to the maximum of the voltages V_{H1} and V_{H2}.

[0051] The double sample amplifier **200** of the PWM controller **100** further includes a current source **285** connected from the output of the signal buffer to the ground reference. This is done in order to pull the signal buffer signal low. To acquire the sampled voltage V_{SH} from the output of the signal buffer, a switch **222** is turned on/off by the sampling pulse V_{SP3}. An input terminal of the switch **222** is connected to the output of the signal buffer. A capacitor **232** for holding the sampled voltage V_{SH} is connected to an output terminal of the switch **222.** The capacitor **232** is further connected to a positive terminal of an operational amplifier **241.** The output of the operational amplifier **241** is connected to a first terminal of a resistor **252.** A second terminal of the resistor **252** outputs the clamped-sample voltage V_{HSH}. A negative terminal of the operational amplifier **241** is connected to the second terminal of the resistor **252.** The operational amplifier **241** keeps the clamped-sample voltage V_{HSH} equal to the sampled voltage V_{SH}, as long as the clamped-sample voltage V_{HSH} is higher than a minimum voltage value V_{MIN}. A current

source **281** is connected to the second terminal of the resistor **252**. The current source **281** and the resistor **252** are used to produce the minimum voltage value V_{MIN} for the clamped-sample voltage V_{HSH}.

[0052] The double sample amplifier **200** of the PWM controller **100** further includes an operational amplifier **240** having a positive terminal connected to a reference voltage terminal V_{RV}. An output of the operational amplifier **240** drives a gate of a transistor **213**. A negative terminal of the operation amplifier **240** is connected to a source of the transistor **213**. The source of the transistor **213** is further connected to the second terminal of the resistor **252** via a resistor **250**. A drain of the transistor **213** is connected to a current mirror. The current mirror comprises a transistor **215** and a transistor **217**. The transistor **215** is an input of the current mirror. A drain of the transistor **217** is connected to a resistor **251**, to produce the feedback voltage V_{COM} at the **COM** input of the PWM controller **100**. In this manner as described above, an error amplifier is provided for the voltage feedback loop of the PWM controller **100**. The resistor **250** determines the gain of the error amplifier, and the capacitor **37** shown in the FIG. **2** determines the bandwidth of the error amplifier.

[0053] The double sample amplifier **200** of the PWM controller **100** further includes a current source **280** and a programmable current generator **290** connected in series. A junction of the current source **280** and the programmable current generator **290** is connected to an input of the offset current source. The offset current source comprises a diode **260**, a transistor **210** and a transistor **211**. A drain of the transistor **210** is the input of the offset current source. To sink the offset current I_M, the detection input **VS** is connected to a drain of the transistor **211**. The programmable current generator **290** generates a programmable current I_T that is inversely proportional to temperature

variation. Therefore, the amplitude of the offset current $\mathbf{I_M}$ is inversely proportional to temperature variation, such that the offset current $\mathbf{I_M}$ decrease in response to temperature increases.

[0054] FIG. **5** shows a preferred embodiment of the programmable current generator **290** that generates the programmable current $\mathbf{I_T}$ in response to temperature variation. The programmable current generator **290** comprises bipolar transistors **291** and **292**, p-mirror transistors **294**, **295** and **296**, n-mirror transistors **297** and **298** and a resistor **293**. The programmable current $\mathbf{I_T}$ is given by,

$$I_T = N_M \times \frac{k \times T_{emp}}{q} \times \frac{\ln(r)}{R_T} \qquad \text{---------- (1)}$$

where $\mathbf{R_T}$ is the resistance of the resistor **293**; $\mathbf{N_M = M_1 \times M_2}$; $\mathbf{M_1}$ is the geometrical ratio of the transistor **295** and **296**; $\mathbf{M_2}$ is the geometrical ratio of the transistor **297** and **298**; **k** is the Boltzmann's constant; **q** is the charge on an electron; **r** is the emitter area ratio of the bipolar transistor **291** and **292**; and $\mathbf{T_{emp}}$ is the absolute temperature.

[0055] FIG. **6** shows a preferred embodiment of the oscillator **300** of the PWM controller **100** according to the present invention. In this embodiment, the clamped-sample voltage $\mathbf{V_{HSH}}$ is supplied to a positive input of an operational amplifier **340**. The operational amplifier **340** is coupled to a transistor **310** and a resistor **360**, to generate a variable charge current $\mathbf{I_{310}}$. A transistor **311** paired with a transistor **312** produce a first discharge current $\mathbf{I_{312}}$ by mirroring the variable charge current $\mathbf{I_{310}}$. The pair of transistors **311** and **314** produces a charge current $\mathbf{I_{314}}$ by mirroring the variable charge current $\mathbf{I_{310}}$. A transistor **315** paired with a transistor **316** produces a second discharge current $\mathbf{I_{316}}$ by mirroring the first discharge current $\mathbf{I_{312}}$. A switch **351** is used to enable and disable the charge current $\mathbf{I_{314}}$. A switch **352** is used to enable and disable the second discharge current $\mathbf{I_{316}}$. The charge current $\mathbf{I_{314}}$ and the second discharge current $\mathbf{I_{316}}$ are supplied to a

capacitor **365**, to generate a saw-tooth signal. A comparator **345**, a comparator **346**, a reference voltage V_2, a reference voltage V_1, a NAND-gate **381**, and a NAND-gate **382**, are coupled to generate a clock signal V_{CLK} to control the switch **352**. The clock signal V_{CLK} also controls the switch **351** via an inverter **380**.

[0056] FIG. **7** shows a preferred embodiment of the PWM circuit **500** of the PWM controller **100** according to the present invention. The PWM circuit **500** comprises a comparator **545**, a comparator **546**, a NAND-gate **510**, a NAND-gate **511**, a flip-flop **515**, an inverter **512**, an AND-gate **519**, and a blanking circuit **520**. A negative input of the comparator **545** and a negative input of the comparator **546** are connected to the current-sense input **IS** of the PWM controller **100**. The comparator **545** is used to compare the feedback voltage V_{COM} with the current-sense voltage V_{IS}. The comparator **546** is used to compare a limit voltage V_{LIMIT} with the current-sense voltage V_{IS}. The limit voltage V_{LIMIT} is used to limit the peak primary current of the transformer **50**. An output of the comparator **545** is connected to a first input of the NAND-gate **510**. An output of the comparator **546** is also connected to a second input of the NAND-gate **510**. A first input of the NAND-gate **511** is connected to an output of the NAND-gate **510**. A second input of the NAND-gate **511** is connected to an output of the blanking circuit **520**. The clock signal V_{CLK} is supplied to a clock input of the flip-flop **515** via the inverter **512**, which is further connected to a first input of the AND-gate **519**. The flip-flop **515** is reset by an output of the NAND-gate **511**. An input of the flip-flop **515** is supplied from the supply voltage V_{CC}. An output of the flip-flop **515** connects to a second input of the AND-gate **519**. An input of the flip-flop **515** is supplied from the supply voltage V_{CC}. An output of the AND-gate **519** supplies the PWM signal V_{PWM} to an input of the blanking circuit **520**. The blanking circuit **520** generates a blanking signal V_{BLK} to ensure a

minimum on-time for the PWM signal V_{PWM}.

[0057] FIG. **8** shows a preferred embodiment of the blanking circuit **520** of the PWM circuit **500** according to the present invention. The blanking circuit **520** comprises an inverter **521**, an inverter **522**, a NAND-gate **523**, a transistor **526**, a capacitor **527**, and a current source **525**. The purpose of the blanking circuit **520** is to generate the blanking signal V_{BLK}. The PWM signal V_{PWM} is supplied to an input of the inverter **521** and a first input of the NAND-gate **523**. The transistor **526** is coupled with the current source **525**, the capacitor **527**, and the inverter **522**, to produce a blanking time T_{BLK}. An output of the inverter **521** drives a gate of the transistor **526** to start the blanking time T_{BLK}, once the PWM signal V_{PWM} is on. An output of the inverter **522** is connected to a second input of the NAND-gate **523**. An output of the NAND-gate **523**, which is an output of the blanking circuit **520**, generates the blanking signal V_{BLK}. Its waveform is shown in FIG. **10**.

[0058] FIG. **9** shows a preferred embodiment of the pulse generator **700** of the PWM controller **100** according to the present invention. To produce a sampling clock signal the pulse generator **700** includes a capacitor **751**, an inverter **736**, a switch **737**, a current source **710**, a current source **711**, and a hysteresis buffer **735**. The capacitor **751** is charged by the current source **710** via the switch **737**, and is discharged by the current source **711**. The capacitor **751** is connected to an input of the hysteresis buffer **735**. The hysteresis buffer **735** outputs a sampling clock signal to control the switch **737** via the inverter **736**. The current source **710** and the current source **711** respectively determine an on-time and an off-time of the sampling clock signal. The on-time of the sampling clock signal further determines the sample time T_{S1} for both of the sampling pulse signals V_{SP1} and V_{SP2}. To produce a delay time T_d after the PWM signal V_{PWM} goes off, the pulse

generator **700** includes a transistor **741**, a current source **712**, a capacitor **752**, an inverter **721**, and an inverter **722**. The PWM signal V_{PWM} is also supplied to an input of the inverter **721**. The output of the inverter **721** drives the inverter **722**. The inverter **722** further drives a gate of the transistor **741**. When the PWM signal V_{PWM} goes off, the transistor **741** is also turned-off. The current source **712** will then charges the capacitor **752** to produce the delay time T_d.

[0059] The pulse generator **700** of the PWM controller **100** further comprises an AND-gate **726** having three inputs. A first input is supplied by the sampling clock signal, a second input is connected to the capacitor **752**, and a third input is connected to the output of the inverter **721**. An output of the AND-gate **726** produces the sampling pulses V_{SP1} and V_{SP2} via an AND-gate **733** and an AND-gate **732** respectively. The AND-gates **732** and **733** are alternately enabled by a flip-flop **731**. The sampling clock signal is supplied to a clock input of the flip-flop **731**. An output and an inverse-output of the flip-flop **731** are connected to the AND-gates **732** and **733** respectively, thus the sampling pulses V_{SP1} and V_{SP2} can be alternately produced. Furthermore, in order to sample the flyback voltage just before the transformer current drops to zero, the ZCD signal V_{ZCD} controls the AND-gates **732** and **733** via an OR-gate **729**.

[0060] However, to ensure that the double sample amplifier **200** will produce the sampled voltage V_{SH} during every switching cycle, the ZCD signal V_{ZCD} disables the sampling pulses V_{SP1} and V_{SP2} after they are produced.

[0061] The inverse-output of a flip-flop **730** connects to a first input of the OR-gate **729**. A second input of the OR-gate **729** is supplied by the ZCD signal V_{ZCD}. The flip-flop **730** is reset by the output of the inverter **721**. A clock input of the flip-flop **730** is connected to the output of the AND-gate **726** via an inverter **725**. Thus, the ZCD signal V_{ZCD} will

disable the AND-gates **732** and **733** following either of the sampling pulses, V_{SP1} or V_{SP2}.

[0062] To produce a sampling pulse V_{SP3} with a pulse width equal to a sample time T_{S2}, the pulse generator **700** includes a transistor **742**, a current source **714**, a capacitor **753**, an inverter **723**, an inverter **724**, and an AND-gate **727**. The clock signal V_{CLK} is supplied to an input of the inverter **723** and a first input of the AND-gate **727**. An output of the inverter **723** is connected to a gate of the transistor **742** to control the start of the sample time T_{S2}. The current source **714** and the capacitor **753** are coupled to produce the sample time T_{S2}. The capacitor **753** drives a second input of the AND-gate **727** via the inverter **724**. The AND-gate **727** outputs the sampling pulse V_{SP3} with a pulse width equal to the sample time T_{S2}.

[0063] FIG. **10** shows the timing diagram of the PWM circuit **500** and the pulse generator **700**. After the PWM signal goes low, the sampling pulses V_{SP1} and V_{SP2} are alternately generated, following the delay time T_d. The purpose of the delay time T_d is to eliminate as much as possible the influence of the leakage inductance of the transformer **50**. To accomplish this, the delay time T_d is inserted during each cycle between the falling-edge of the PWM signal V_{PWM} and the beginning of the flyback voltage sampling process. The blanking circuit **520** shown in FIG. 7 produces the blanking time T_{BLK}. This determines the minimum on-time of the PWM signal, once the PWM signal is on. The delay time T_d is determined by the minimum on-time of the PWM signal. The blanking time T_{BLK} ensures that the delay time T_d and the sample time T_{S1} and T_{S2} are sufficient to precisely sample the flyback voltage. When a zero current status is detected at the detection input VS, both the sampling pulses V_{SP1} and V_{SP2} will be disabled. The flyback voltage will be sampled and held by the capacitors **230** and **231**, depicted in FIG. **4**. The sampling pulse V_{SP3} is then generated in response to the clock signal V_{CLK}. When the

sampling pulse $\mathbf{V_{SP3}}$ is generated, the capacitor **232** will further sample and hold the higher voltage stored by the capacitors **230** or **231**. Referring now to FIG. **2**, the output voltage $\mathbf{V_O}$ of the power converter can be expressed as,

$$V_O = V_{NS} - V_D = \frac{N_S}{N_{P1}} \times V_{P1} - V_D = \frac{N_S}{N_{P1}} \times (V_{SH} + I_M \times R_{23}) - V_D \quad \text{---------- (2)}$$

where $\mathbf{V_{NS}}$ is the voltage across the secondary winding $\mathbf{N_S}$, $\mathbf{V_{P1}}$ is the voltage of the first primary winding, $\mathbf{V_D}$ is the voltage drop across the output rectifier **19**, $\mathbf{V_{SH}}$ is the voltage sampled at the detection input **VS**, and $\mathbf{R_{23}}$ is the resistance of the detection resistor **23**. The output voltage $\mathbf{V_O}$ can also be expressed in terms of the PWM feedback-control circuit:

$$V_O = G_M \times (V_{RV} - V_{SH}) \quad \text{---------- (3)}$$

where $\mathbf{G_M}$ is the loop gain of the PWM feedback-control circuit and $\mathbf{V_{RV}}$ is the reference voltage of the double sample amplifier **200**. Based on equations (2) and (3), the output voltage can be rewritten as,

$$V_O = \{\frac{N_S}{N_{P1}} \times V_{RV} + [(\frac{N_S}{N_{P1}} \times I_M \times R_{23}) - V_D]\} \div \{1 + (\frac{N_S}{N_{P1}} \times \frac{1}{G_M})\}$$

Because $\mathbf{G_M} >> 1$, $\mathbf{V_O}$ can be expressed in a simplified form as,

$$V_O = \frac{N_S}{N_{P1}} \times V_{RV} + [(\frac{N_S}{N_{P1}} \times I_M \times R_{23}) - V_D] \quad \text{---------- (4)}$$

[0064] The flyback voltage is sampled just before the transformer current drops to zero. The problem is that the voltage drop across the output rectifier **19** varies with respect to temperature.

[0065] To compensate for this, the present invention introduces the offset current $\mathbf{I_M}$. The offset current $\mathbf{I_M}$ is modulated in inverse proportion to temperature variation. By properly selecting the resistance of the detection resistor **23**, it is possible to offset the

adverse temperature effect of the voltage drop across the output rectifier **19**. Thus, the flyback power converter according to the present invention can supply a well-regulated output voltage V_O.

[0066] The oscillator **300** produces the clock signal V_{CLK} with a programmable switching frequency. The switching frequency is determined in response to the clamped-sample voltage V_{HSH}. This controls the power delivered from the primary-side of the transformer to the output of the power converter. Because the clamped-sample voltage V_{HSH} is correlated to the output voltage V_O, the switching frequency will be proportional to output voltage V_O. Using the programmable switching frequency, the flyback power converter according to the present invention can maintain a constant output current I_O.

[0067] Since the output power is a function of the output voltage V_O, a constant current output can be achieved when the output current of the power converter is always less than a maximum value. The output power P_O is given by,

$$P_O = Vo \times Io = \eta \times P_{IN} = \eta \times \frac{1}{2 \times T} \times L_P \times I_P{}^2 \quad \text{---------- (5)}$$

where **PIN** is the power input to the primary-side, η is the power conversion efficiency, **T** is the switching period, L_P is the primary inductance of the transformer **50**, and I_P is the primary current of the transformer **50**.

[0068] The primary current I_P produces the current-sense voltage V_{IS} across the current-sense resistor **25**. The current-sense resistor **25** is connected to the current-sense input **IS** of the PWM controller **100**. Once the current-sense voltage V_{IS} exceeds the limit voltage V_{LIMIT}, the logic circuit of the PWM controller **100** will turn off the PWM signal to keep the primary current I_P constant. Referring to equation (5), the output current I_O of the power converter can be shown as,

$$Io = \frac{1}{Vo} \times \frac{\eta}{2 \times T} \times L_P \times (I_P)^2 \quad \text{---------- (6)}$$

[0069] In order to produce a constant output current $\mathbf{I_O}$, when $V_{O2} = 0.5 \times V_{O1}$ ($P_{O2} = 0.5 \times P_{O1}$), **T** should be increased as follows:

$$T_2 = 2 \times T_1$$

where the first switching period $\mathbf{T_1}$ refers to the first output voltage $\mathbf{V_{O1}}$, and the second period of the switching frequency $\mathbf{T_2}$ refers to the second output voltage $\mathbf{V_{O2}}$.

[0070] The oscillator **300** generates the clock signal $\mathbf{V_{CLK}}$ with a programmable switching frequency. The switching frequency is determined in response to the clamped-sample voltage $\mathbf{V_{HSH}}$. When the clamped-sample voltage $\mathbf{V_{HSH}}$ exceeds the minimum voltage $\mathbf{V_{MIN}}$, the clamped-sample voltage $\mathbf{V_{HSH}}$ is equal to the sampled voltage $\mathbf{V_{SH}}$. If the clamped-sample voltage $\mathbf{V_{HSH}}$ goes below the minimum voltage value $\mathbf{V_{MIN}}$, the switching frequency of the oscillator **300** will be insufficient to operate the PWM controller **100**. To prevent this from happening, the clamped-sample voltage $\mathbf{V_{HSH}}$ will be set to the minimum voltage value $\mathbf{V_{MIN}}$, whenever it starts to dip below $\mathbf{V_{MIN}}$.

[0071] Referring to equation (2), the sampled voltage $\mathbf{V_{SH}}$ is per se a function of the output voltage $\mathbf{V_O}$. Therefore a constant output current can be easily achieved by reducing the switching period to (2 × T), whenever the output voltage is decreased to (0.5 × $\mathbf{V_O}$).

[0072] As described above, the flyback power converter includes the PWM controller **100**, to generate the offset current $\mathbf{I_M}$ and the sampled voltage $\mathbf{V_{SH}}$. The sampled voltage $\mathbf{V_{SH}}$ is generated during every PWM cycle in response to the flyback voltage sampled across the first primary winding. In this manner, the flyback power converter according to the present invention can keep the output voltage constant. To limit the power

transferred through the primary winding, the switching frequency is generated in response to the output voltage V_O. In this manner, the flyback power converter according to the present invention keeps the output current constant.

[0073] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.